

# Dual Voltage Tracking Circuit for I/O, Microprocessor, and DSP Core Voltages

*This note describes a dual tracking controller for a single I/O voltage and two core voltages. It describes how to apply the circuit to one or many core voltages.*

*Principles covered include: the need for tracking, practical circuits, controller functions, selection of tracking voltage levels, component value selection, overall circuit accuracy, circuit stability, the characteristics of some commercially-available DC/DC converters, and cascaded supply and parallel supply operation. Circuits are provided with options and tracking waveforms.*

[\*A component-selection spreadsheet for calculating component values\*](#)

*(Excel, 196KB) is available*

## Voltage Tracking Requirements

It is important that a microprocessor's input/output (I/O) and core voltages not depart from a manufacturer's specifications at power-up and power-down. A typical contemporary microprocessor's I/O section usually operates at 3.3V or 2.5V, while the core may operate at 1.8V, 1.5V or 1.3V. Typical requirements are that the core and I/O voltages not differ from one another more than a small specified amount during power up/down, and that the voltages not be out of tolerance longer than a few tens of milliseconds during power up or power down. Guidelines on the PowerPC™, for example place a 20ms limit on out-of-tolerance I/O and core voltages at power up/down and a  $\pm 50\text{mV}$  spec on core voltage. The latter spec, incidentally, suggests better than  $\pm 2.8\%$  supply accuracy (including any series tracking-circuit voltage drop) at 1.8V.

## Voltage Tracking Methods

Several methods are in use to satisfy the power-up/down tracking requirements: Schottky-diode matrix circuits, multi-channel series tracking circuits, and shunt tracking circuits. While series tracking exhibits series voltage/power loss, diode matrices require complex diode selection and a diode can blow under short circuit conditions, shunt tracking has neither drawback. The MAX5039 and MAX5040 shunt tracking controllers not only eliminate series voltage/power loss but minimize tracking-circuit component count to contribute to a lowest-cost solution. Only one MOSFET is required (per core voltage) to effect tracking of I/O and core voltages, and this MOSFET is active for only a few milliseconds during power-up/down.

## Basic Circuit Description

The basic dual shunt voltage-tracking controller circuit of Figure 1 employs a single MAX5039 tracking controller and a single NMOS device for each core voltage in the system. Each NMOS is controlled to connect the I/O- and CORE-voltage lines ( $V_{I/O}$  and  $V_{CORE}$ ) together during the power up/down periods. Each controller and MOSFET acts as a series-voltage regulator only briefly during the tracking phases at power up/down so power dissipation is minimal and occurs for only a few milliseconds per power cycle. No series-circuit voltage drop or power dissipation occurs in normal operation.

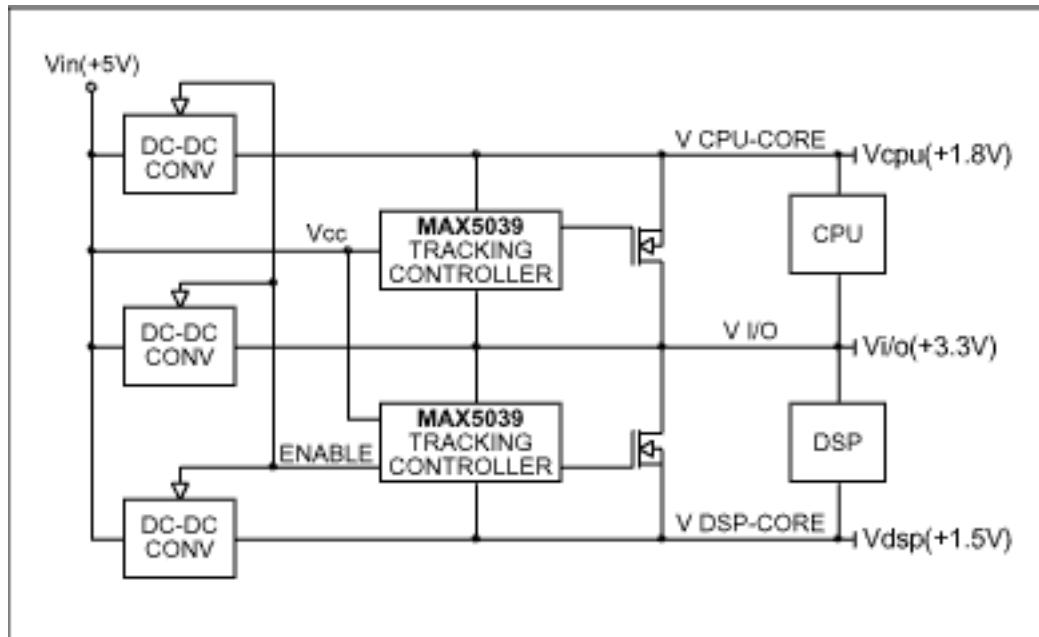


Figure 1. Basic Dual Voltage-Tracking Control.

When  $V_{I/O}$  comes up before  $V_{CORE}$ ,  $V_{CORE}$  is derived from the higher  $V_{I/O}$  voltage with the controller and MOSFET operating as a series regulator. When  $V_{CORE}$  comes up before  $V_{I/O}$ , the  $V_{I/O}$  is connected to the  $V_{CORE}$  voltage with the controller and MOSFET operating as a series switch. It may be preferable that the  $V_{I/O}$  supply come up slightly before the  $V_{CORE}$  supply, but it is not a requirement (depends upon supply characteristics).

## Detailed Circuit

A complete single-channel voltage-tracking circuit with all options appears in Figure 2. This circuit contains the full-featured MAX5040 providing a power-OK or POK output. The open-drain POK output is released to go HIGH when the voltage at I/O SENSE  $\leq 1.230V$  and the tracking phase is completed.

The component functions are as follows:

- MAX5040 - tracking controller
- Q1, NMOS - shunt switch or regulator
- C1, C2 & R3 - regulator control-loop compensation

- R1 & R2 - feedback voltage-control attenuator sets  $V_{CORE}$  tracking voltage
- R9 & C3 - feedback lead network
- R5/R6 - power-OK sense setpoint attenuator
- D1 & CIN - energy storage allows controller to continue functioning while power shuts down
- R7 & R8 - startup-voltage setpoint attenuator.

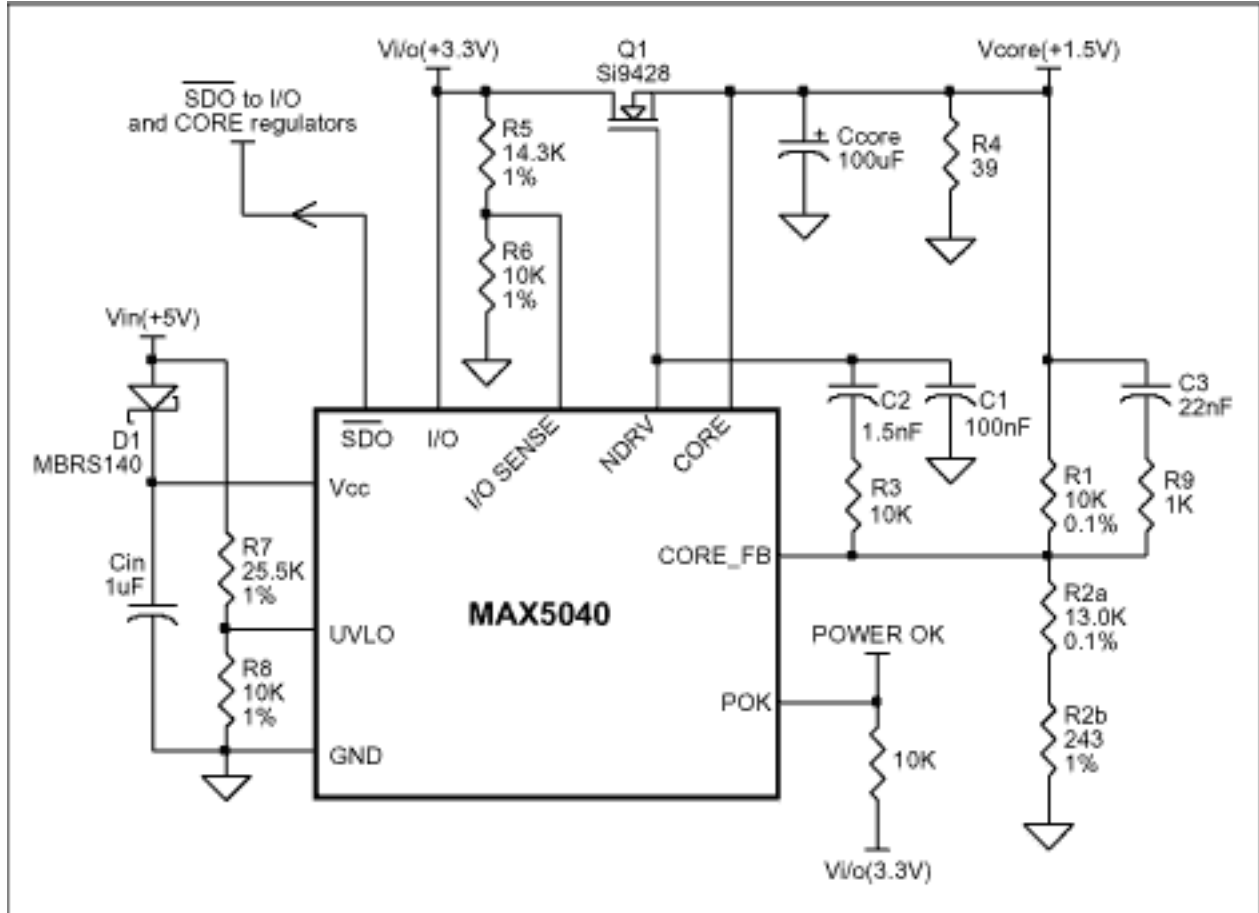


Figure 2. Complete Voltage Tracking Circuit for a Single Core Voltage.

## Detailed Dual Tracking Control Circuit

The single  $V_{CORE}$  tracking controller of Figure 2 is extended to multiple  $V_{CORE}$  systems simply by including one additional controller/MOSFET circuit for each additional  $V_{CORE}$  that requires tracking. A complete dual tracking circuit appears in Figure 3.

Note that only a single UVLO resistor divider is used. The /SDO\ output of the first controller is connected to the UVLO input of the next controller in daisy-chain manner, and /SDO\ of the final controller in the series is used to enable all low-voltage regulators. Each R1/R2 divider is adjusted for the required tracking core voltage. If MAX5040 controllers are used, each POK output may be used independently or collector ORed to provide a single composite POK if desired. Otherwise, a single MAX5040 could be used while the remaining controllers are MAX5039.

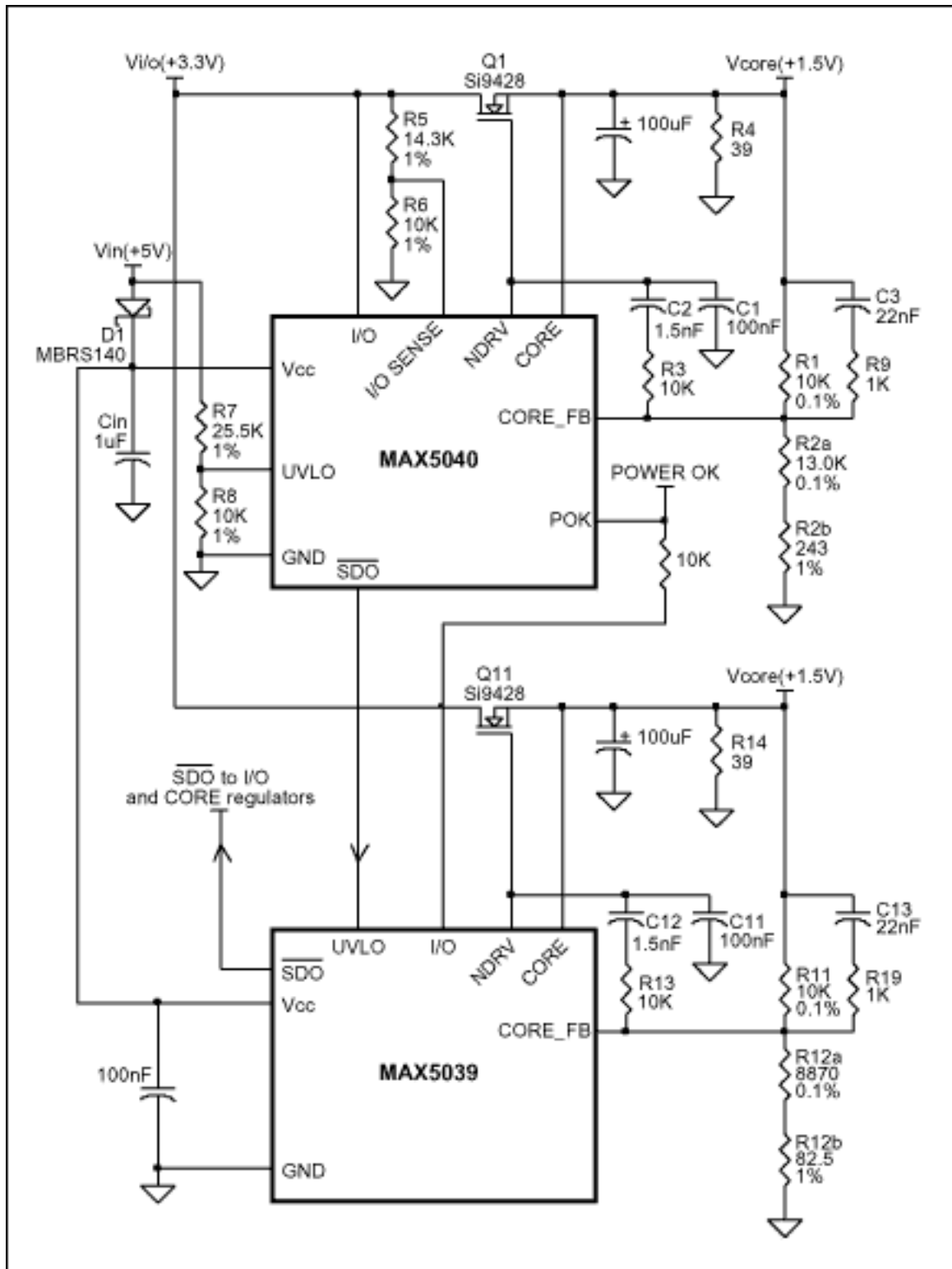


Figure 3. Dual Tracking Controller Circuit for Two Core Voltages.

### Controller Turn-On Operation

The MAX5039/MAX5040 tracking controller is powered by V<sub>CC</sub> from a 5V control supply line. The following explanations assume that the V<sub>I/O</sub> enable signal precedes the V<sub>CORE</sub> enable signal. [Differences are noted for situations when the two enable signals are coincident or when V<sub>CORE</sub> enable precedes V<sub>I/O</sub> enable.]

1. Startup operation is initiated when  $V_{CC}$  is applied (either ramped or stepped up from zero). Refer to Figure 4.
2. The IC becomes active when  $V_{CC}$  reaches 0.9V, at which time the active-low regulator-shutdown line  $\overline{SDO}$  is driven LOW to insure that the  $V_{I/O}$  and  $V_{CORE}$  supply regulators are disabled.
3. When  $V_{CC}$  reaches 2.5V, NDRV is driven to  $V_{CC}$ , turning ON the low-threshold MOSFET to connect the  $V_{I/O}$  and  $V_{CORE}$  lines together. The supply regulators are still OFF because  $\overline{SDO}$  remains LOW.
4. When  $V_{CC}$  reaches  $\approx 4.5V$  (set the R7/R8 undervoltage-control attenuator so that the UVLO pin reaches 1.230V at this point),  $\overline{SDO}$  is driven HIGH to enable the  $V_{I/O}$  and  $V_{CORE}$  supply regulators. The  $V_{I/O}$  and  $V_{CORE}$  supply regulator outputs remain connected together through the MOSFET as NDRV remains at  $V_{CC}$ .
5.  $V_{I/O}$  precedes  $V_{CORE}$ , and begins to rise at a rate determined by the I/O regulator characteristics. NOTE: Neither  $V_{I/O}$  nor  $V_{CORE}$  should rise at a rate exceeding  $6.6V/\mu s$ .  $V_{CORE}$  rises with  $V_{I/O}$  because the two regulator output lines are connected via the MOSFET. During this phase, the I/O regulator output supplies both the I/O and CORE loads and backdrives the CORE regulator output; both voltages are equal. [If  $V_{CORE}$  precedes  $V_{I/O}$ ,  $V_{CORE}$  backdrives the  $V_{I/O}$  supply; both voltages are equal. Refer to Figure 5.]

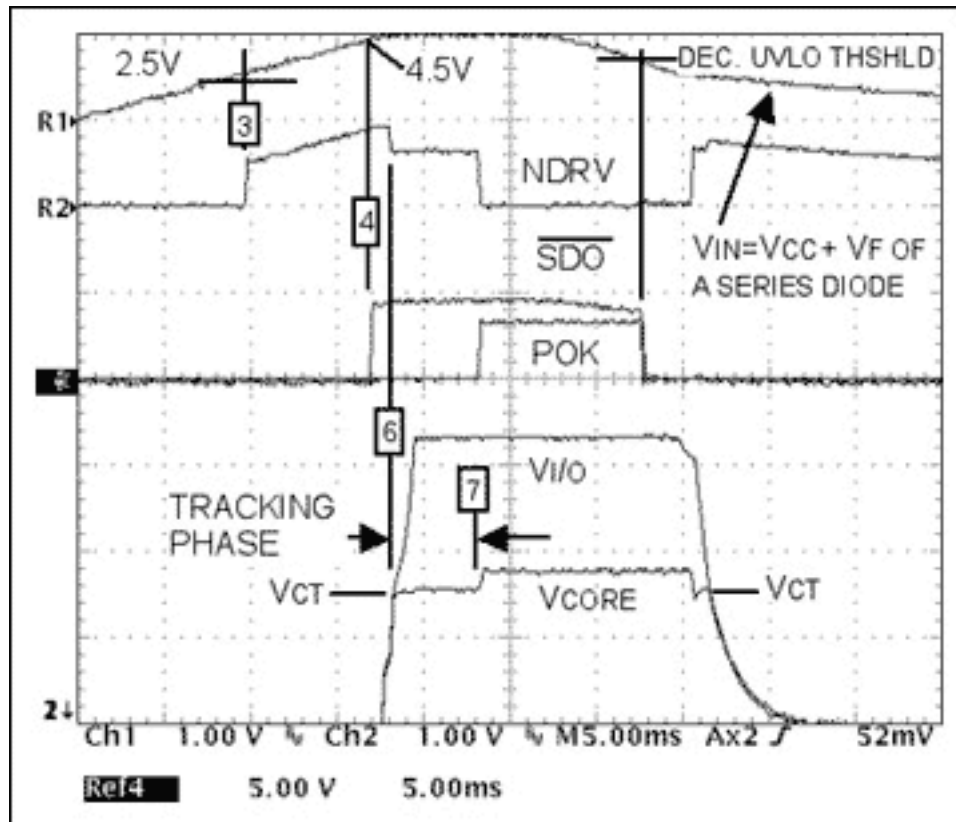


Figure 4. Startup/Shutdown Operation,  $V_{I/O}$  Enable Precedes  $V_{CORE}$  Enable.

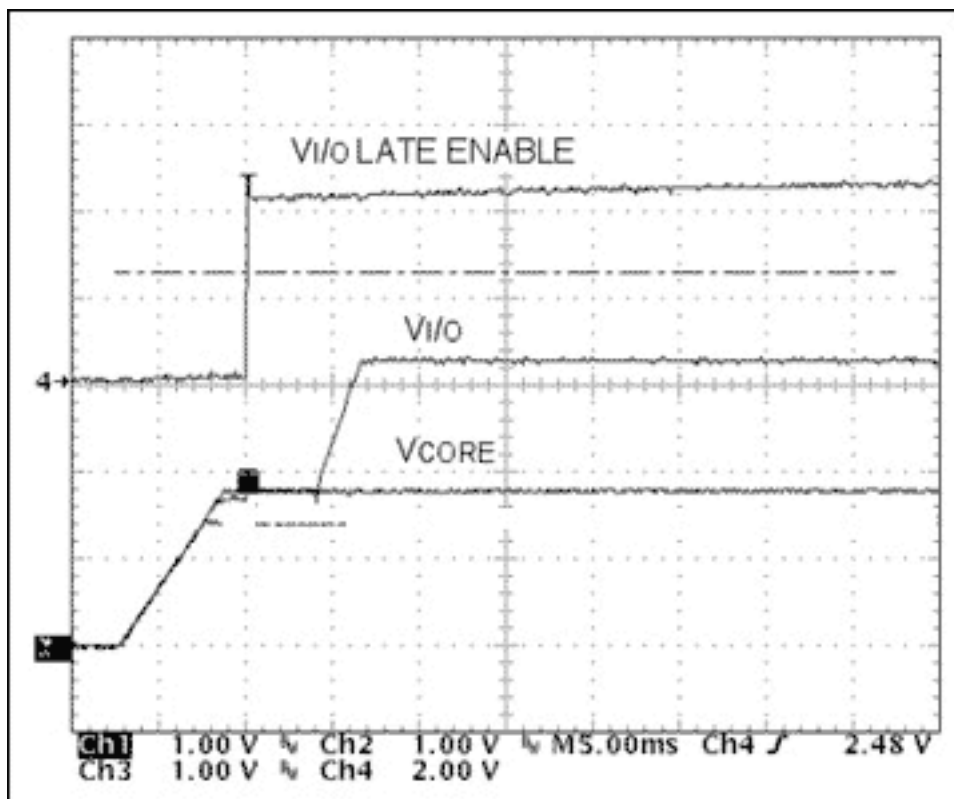


Figure 5. Startup Operation,  $V_{CORE}$  Enable Precedes  $V_{I/O}$  Enable.

6. When  $V_{CORE}$  ( $=V_{I/O}$ ) reaches the programmed  $V_{CORE}$  set point, NDRV drops from  $V_{CC}$  to a lower value as necessary to regulate  $V_{CORE}$  at the pre-selected set point slightly below its normal value. [If  $V_{CORE}$  precedes  $V_{I/O}$ , the set point is ignored,  $V_{CORE}$  rises to its normal regulator-controlled level,  $V_{I/O}$  equals  $V_{CORE}$  until the I/O regulator output is available and  $V_{I/O}$  exceeds  $V_{CORE}$ . At this time NDRV is driven LOW to turn OFF the MOSFET, the two voltages become independent,  $V_{I/O}$  rises to its normal level, POK is released to go HIGH, and the controller turn-on sequence is terminated.]

7. The controller and MOSFET act as a series-pass regulator until  $V_{CORE}$  becomes available when  $V_{CORE}$  rises to its normal regulator-controlled level, NDRV is driven LOW to turn OFF the MOSFET, the two voltages become independent,  $V_{I/O}$  rises to its normal level, and the controller turn-on sequence is terminated.

8. If the turn-on sequence is delayed because either  $V_{I/O}$  or  $V_{CORE}$  does not come up within an internally-timed 15ms after  $/SDO\$  is released,  $/SDO\$  will be driven LOW to abort the turn-on sequence. This fault condition is latched to prevent an automatic restart attempt.

## Controller Turn-Off Operation

CORE drops to the core regulation voltage set by R1/R2 (perhaps due to an unexpected high-current load or a short), NDRV will be driven high to re-assert the regulation mode. Refer to Figure 4.

If this condition lasts beyond the 10-20ms fault time - or if the voltage on the UVLO pin drops below its threshold voltage,  $/SDO\$  will be driven LOW to begin a shutdown operation.

1.  $V_{UVLO}$  drops below the UVLO threshold, or a fault lasts beyond 10-20ms.
2.  $/SDO$  is driven LOW to disable the  $V_{I/O}$  and  $V_{CORE}$  supplies.
3. An internal 20W MOSFET bleeder between  $V_{CORE}$  and ground is turned ON to discharge the output loads.
4.  $V_{CORE}$  begins to drop.
5.  $V_{CORE}$  drops to the  $V_{CORE}$  set point while  $V_{I/O}$  remains higher than  $V_{CORE}$ , NDRV is driven to an intermediate point as needed to regulate  $V_{CORE}$  at the set point so long as  $V_{I/O}$  remains greater than  $V_{CORE}$ .
6.  $V_{I/O}$  drops to  $V_{CORE}$ , NDRV is driven to  $V_{CC}$ , turning ON the MOSFET to short the  $V_{I/O}$  and  $V_{CORE}$  lines together. Note: It is important that  $V_{CC}$  remain in its operating range during the power-down stage so that the controller can continue to control NDRV until the loads are discharged<sup>[1]</sup>.

## Selecting the Core-Voltage Tracking Level

The core-voltage tracking level<sup>[2]</sup>  $V_{CT}$  - set by feedback attenuator R1/R2 in Figure 2 - is that voltage at which  $V_{CORE}$  is held while the controller is in tracking mode. This occurs when the  $V_{I/O}$  supply comes up before the  $V_{CORE}$  supply. Selection of the core-voltage tracking level is an important consideration that depends primarily upon the  $V_{CORE}$  and  $V_{I/O}$  supply accuracies. The constraints are as follows:

- $V_{CT}$  must be below the tolerance-limit value of  $V_{CORE}$ ,
- $V_{CT}$  must be above  $V_{I/O}$  minus the allowed differential between  $V_{I/O}$  and  $V_{CORE}$ ,
- $V_{CT}$  cannot be above  $V_{I/O}$ , or
- $V_{CT}$  must be above the minimum allowed  $V_{CORE}$ .

We must know in advance the limits on the  $V_{I/O}$  and  $V_{CORE}$  supplies.

As an example, we set the following limits:

$V_{I/O}$  supply =  $3.3V \pm 5\%$ , or 3.135-3.465V,

$V_{CORE}$  supply =  $1.5V \pm 50mV$  ( $\pm 3.33\%$ ), or 1.45-1.55V,

$V_{CORE}$  minimum voltage =  $1.5V - 10\%$ , or 1.35V, and

$V_{CT}$  must then be in the range 1.35-1.45V including all setting errors.

Attenuator R1/R2 ratio is chosen such that 0.8V appears on the CORE\_FB pin during the tracking phase. We will use  $V_{CT} = 1.40V$  in the example.

Core voltage and  $V_{CT}$  error limits of from all sources are shown in Figure 6. The  $V_{CT}$  must be

kept above 1.35V minimum  $V_{CORE}$  allowed and below 1.45V minimum  $V_{CORE}$  supply range.

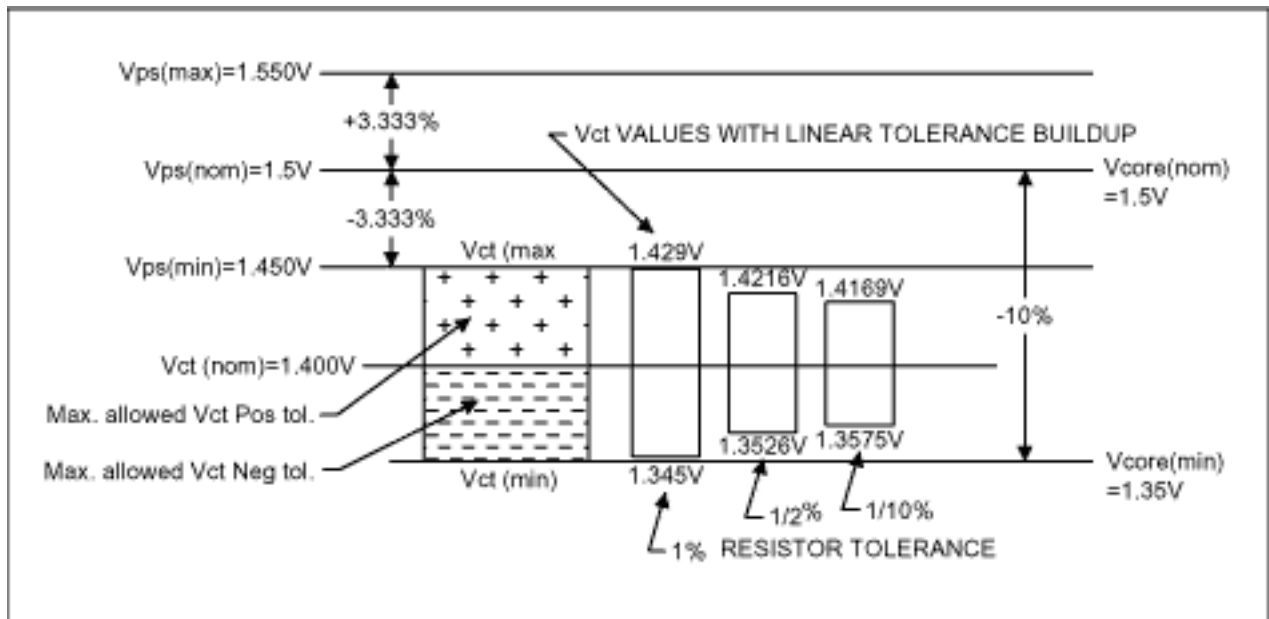


Figure 6. Representation of  $V_{CT}$  Error Limits and Realized Values.

## Determining the Errors

Several errors are associated with setting the voltage at CORE\_FB. They are:

1. The 800mV reference against which the voltage at CORE\_FB is compared has a tolerance of  $\pm 2\%$  over temperature.
2. The resistors themselves have tolerance; suggested resistor tolerance is  $\pm 0.1\%$ .
3. The resistors have a temperature coefficient,  $\pm 25\text{ppm}/^\circ\text{C}$  for 0.1% and 0.5% resistors and  $\pm 100\text{ppm}$  for 1% resistors.
4. Resistor selection may only be made in 1-2% increments.
5. CORE\_FB bias current could have an effect if R1 and R2 are of very high value.
6. The internal control amplifier has a limited gain, so the calculation of R1/R2 ratio includes the effects of finite amplifier open-loop gain. The complex calculation can be ignored in selecting R1/R2, and an error term can be derived.

## But, Don't Panic

We can simplify all of this for you and mechanize the process of selecting R1/R2 values. Actually, the prime contribution to error is the  $\pm 2\%$  of the reference itself. So let's inspect each item, one at a time to see how much each contributes to the total error. All resistor-value related errors are influenced by the R1/R2 ratio so vary with the selected  $V_{CT}$ . The MAX5039/MAX5040 Component-Selection Spreadsheet

<http://pdfserv.maxim-ic.com/arpdf/MAX5039/vset.zip>

performs all error calculations at any allowed R1/R2 ratio; it also mechanizes selection of the UVLO and I/O sense resistor attenuators (see Figure 2).



Many readers may prefer to skip over the following section as it is presented primarily as an aid to understanding how the Component-Selection Spreadsheet is mechanized.

### 1. Reference Error

This is a real  $\pm 2\%$  and cannot be reduced.

### 2. Resistor Tolerance

Resistor tolerance error is not a fixed value independent of the R1/R2 ratio, but is a function of this ratio. Using  $\pm 1\%$  resistors is not recommended. Using  $\pm$  % resistors is similar in cost to using  $\pm 0.1\%$  resistors, so  $\pm 0.1\%$  resistors are recommended. Calculated worst-case tolerance errors are  $\pm 0.0857\%$  at  $V_{CT}=1.40V$  ( $\beta = 0.57143$ ).

$$\%ERROR_{RES-TOL} = \%RESISTOR\_TOLERANCE \times 2(1 - \beta)$$

$$\text{Where: } \beta = \text{feedback\_factor} = \frac{V_{c\_ref}}{V_{cr}} = \frac{800mV}{V_{cr}} = \frac{R_2}{R_1 + R_2}$$

### 3. Resistor TCR

The TCR is stated as  $\pm$  and shown as a typical butterfly curve, so worst case is when one resistor exhibits a positive TCR while the other exhibits a negative TCR. In fact, resistors of equal value would be expected to exhibit nearly identical TCR; and the values of R1 and R2 will differ by less than 2:1. Assuming that similar valued resistors will track to  $\pm 10\text{ppm}$ , calculated worst-case TCR errors for  $\pm 25\text{ppm}$  resistors over a temperature range of  $-40$  to  $+85^\circ\text{C}$  are  $\pm 0.056\%$  at  $V_{CT}=1.40V$ . The spread sheet, however, accepts  $\pm 25\text{ppm}$  as a real value for  $0.1\%$  resistors ( $\pm 0.1398\%$  over temperature at  $1.40V$ ). Resistor TCR error may be calculated according to the formula:

$$\%ERROR_{RES-TCR} = 100 \left[ \beta \left[ 1 + \frac{R_2 [1 + (TCR \times \Delta T)]}{R_1 [1 - (TCR \times \Delta T)]} \right] - 1 \right]$$

TCR is expressed in parts per million, but should be written as a decimal fraction in the equation (e.g.;  $25\text{ppm} = 0.000025$ ).  $\Delta T$  is the absolute value of the greatest difference from  $25^\circ\text{C}$  (e.g.;  $-40$  to  $+85^\circ\text{C}$  yields two values:  $-65^\circ$  and  $+60^\circ$ ).

A similar value applies when the (+) and (-) are reversed in the above quotient.

### 4. Resistor Selection

Although available resistor values are in  $\approx 2\%$  increments, the actual R1/R2 ratio may be made to closely approach the calculated value by the act of splitting R2 into two sections. One section, R2a, is the nearest available value below the calculated value; and the other section, R2b, is a very low value. When handled in this manner, the selection error is normally  $< \pm 0.01\%$  if resistors

are in the E96 sequence or  $\pm 0.05\%$  if in the E24 sequence.

### 5. CORE\_FB Bias Current

The data sheet listing of 300nA max over temperature is selected to allow a short test time, and does not represent the actual leakage current, which is less than 30nA at 85° C. One to thirty nanoamp flowing in R1 (10K) (refer to Figure 7) would cause an error of 10-300 $\mu$ V (+0.0007 to +0.021% of  $V_{CT}$ ), so may be ignored in the error calculation. No negative error is possible in this calculation.

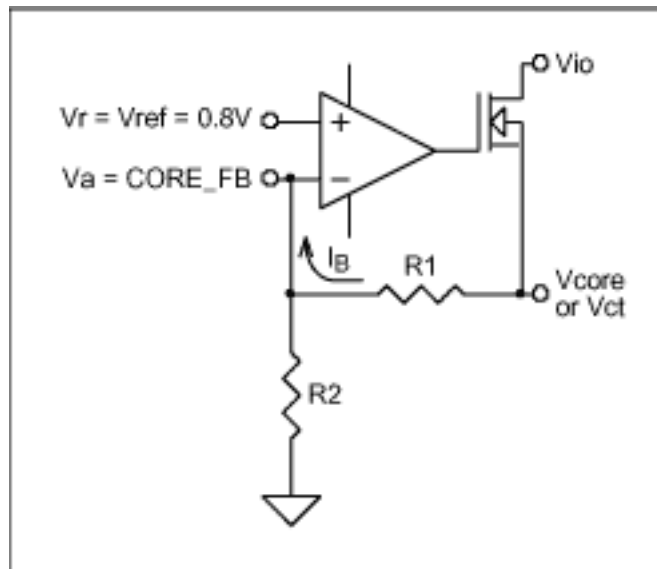


Figure 7. Tracking-Voltage Control Loop.

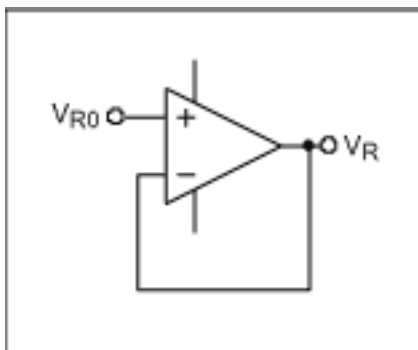


Figure 8. Reference Voltage Measurement Circuit.

### 6. Control Amplifier Open-Loop Gain Limitation

Closed-loop-gain error calculation is somewhat elusive in this case because the given reference-voltage error includes its own loop-gain error due to being measured at the op-amp output when set at unity closed-loop gain. Actual open-loop gain of the op-amp itself is typically 4000, but ranges from 1000 to 10,000<sup>[4]</sup>. The MOSFET source-follower gain is  $\geq 0.99$  due to the extremely high NMOS  $g_{fs}$ , so overall loop gain is nearly unchanged. Normally the closed-loop loop gain of the circuit in Figure 7 is calculated as:

$$A_{VCL} = \frac{V_{CT}}{V_{REF}} = \frac{A_{VOL}}{1 + \beta A_{VOL}}$$

where  $A_{VOL}$  is amplifier open-loop voltage gain and  $\beta$  is the voltage feedback factor.

Appropriate mathematical manipulations can be applied to show that, due to the  $V_{REF}$  measurement and specification method used in Figure 8 where  $V_{REF}$  is measured as  $V_R$ , but is suggested to be located at  $V_{R0}$ , the corrected gain equation is:

$$A_{VCL} = \frac{V_{CT}}{V_R} = \frac{1 + A_{VOL}}{1 + \beta A_{VOL}}, \text{ and } V_{CT} = V_R \frac{1 + A_{VOL}}{1 + \beta A_{VOL}} = V_R \times \frac{\frac{1}{A_{VOL}} + 1}{\frac{1}{A_{VOL}} + \beta}$$

Error can be calculated by forming a ratio of actual to ideal, subtracting 1, and multiplying x100 for percentage. The final form of the  $V_{CT}$  equation above collapses to  $1/\beta$  when  $A_{VOL} = \infty$ , therefore the error at minimum gain is:

$$\% \text{ ERROR}_{\text{calc}} = 100 \left( \frac{\beta(1 + A_{VOL})}{1 + \beta A_{VOL}} - 1 \right) = 100 \left( \frac{1001\beta}{1 + 1000\beta} - 1 \right)$$

Real calculated worst-case open-loop gain error is -0.00075 to -0.0749% at  $V_{CT}=1.40V$ . No positive error is possible in this calculation.

## 7. Error Linear Sum

Calculated worst-case error sum with 0.1% resistors (including 300 $\mu$ V CORE\_FB bias error, 25ppm TCR, and 0.01% resistor-selection error) is -2.316/+2.257% at  $V_{CT}=+1.40V$ . The MAX5039/MAX5040 Component-Selection Spreadsheet calculations include all possible errors except the CORE\_FB bias-current error.

## Circuit Stability Considerations

Components C1, C2, and R3 in Figure 2 control the tracking regulator amplifier stability, and are fully described in the MAX5039/MAX5040 data sheet. It is suggested that the feedback resistor R1 be chosen as a constant value (with adjustment provided by variation of R2). This allows C2 and R3 to remain fixed in value without regard to the  $V_{CT}$  value selected<sup>[5]</sup>. The Component-Selection Spreadsheet calculates these values for any chosen value of R1.

Lead network C3/R9 improves tracking-loop speed to eliminate  $V_{CT}$  overshoot and undershoot during the tracking phase. Figures 9 and 10 illustrate the improvement with the lead network in place. Note the NDRV slow response and overshoot without the lead network and the resultant

$V_{CT}$  overshoot and undershoot in Figure 9 (vertical scales differ in the two figures). The Component-Selection Spreadsheet calculates these values for any chosen value of R1.

Resistor R4 may remain fixed without regard to the value of  $C_{CC}$  when the lead network is in place. R4=39 $\Omega$  works well with  $C_{CC}$  values to 1500 $\mu$ F or more. For very large values of  $C_{CC}$ , one might consider reducing R4 for slightly-improved loop stability in the tracking phase.

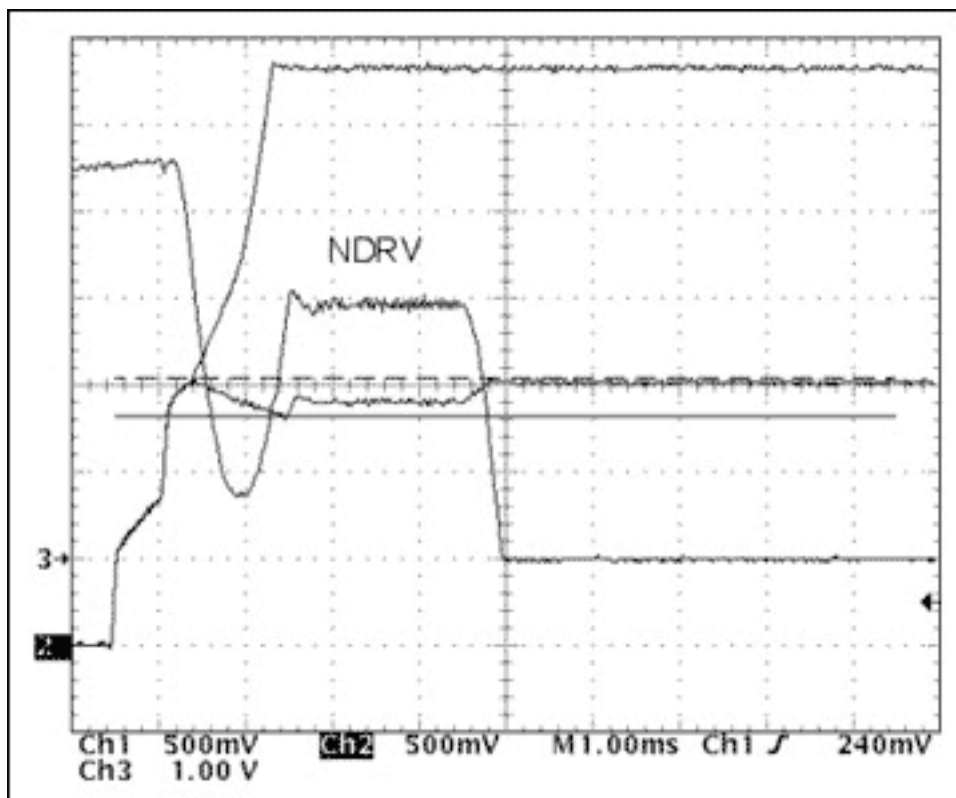


Figure 9. Startup Waveforms without Lead Network.

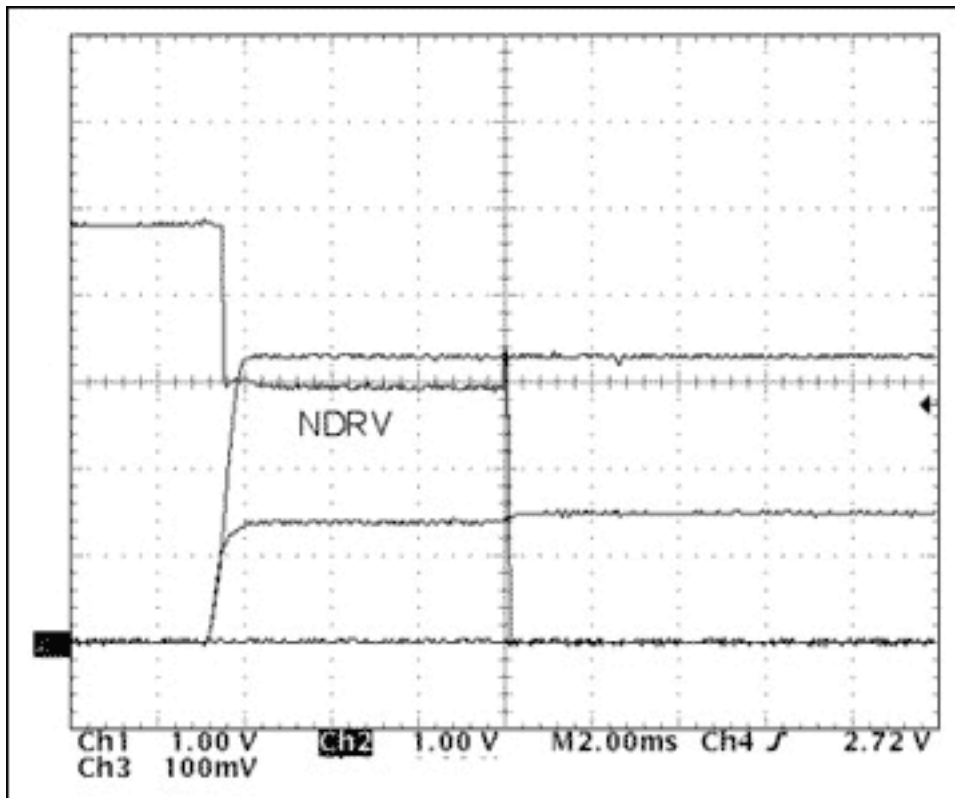


Figure 10. Startup Waveforms with Lead Network.

Dual-tracking-control startup and shutdown waveforms appear in Figures 11 & 12.

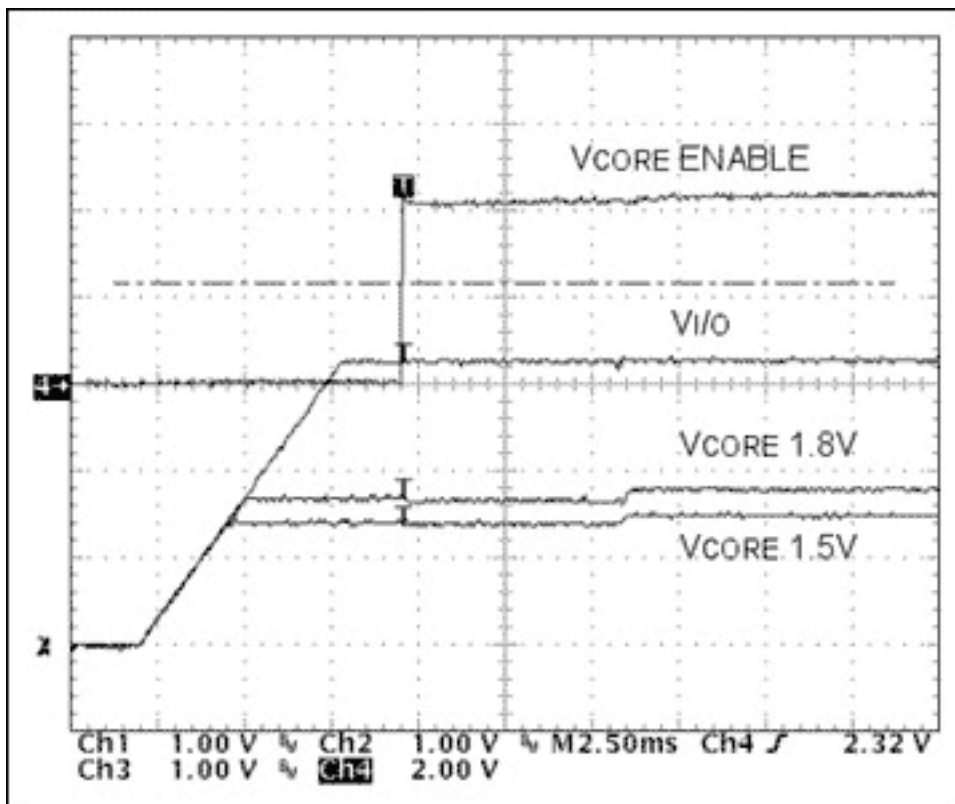


Figure 11. Dual Tracking Startup Waveforms.

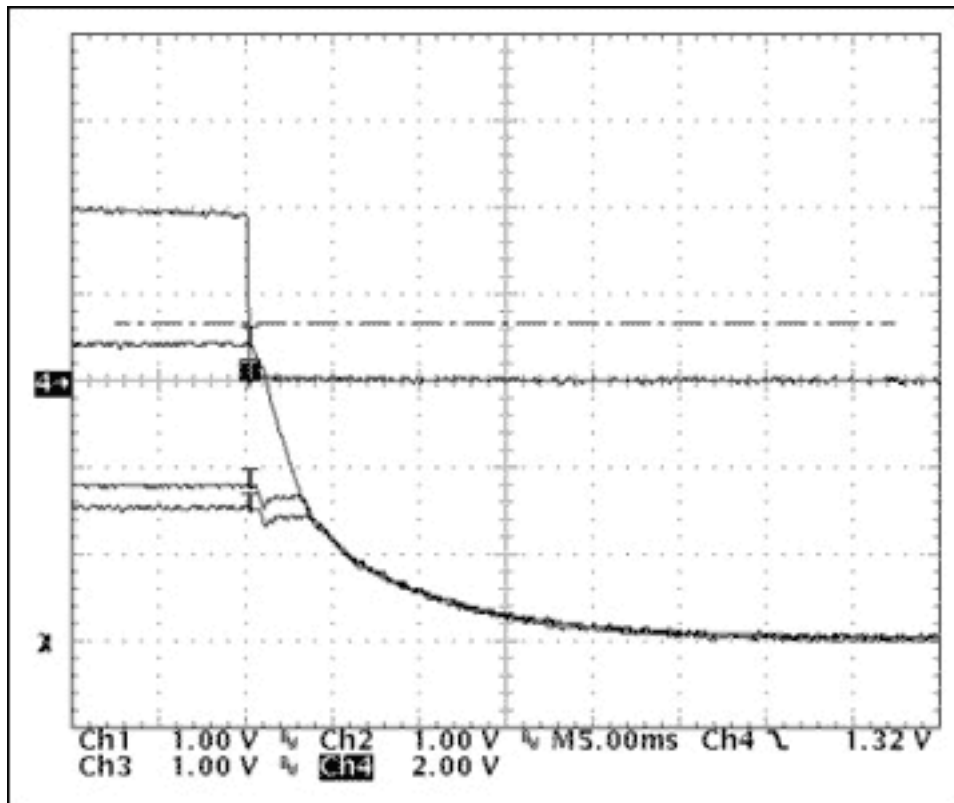


Figure 12. Dual Tracking Shutdown Waveforms.

## Special Considerations - Power-System Source Configurations

Individual system designs will have different power supply and power regulator/converter configurations. Whereas one power system may have a single 5V source of power available to feed all of the low-voltage converters required by the system, another power system may have a single 3.3V power source. Still others may have the several I/O and CORE voltages available from a single multi-voltage source without enable control lines. Each will benefit from a variation in the tracking circuit configuration.

We will consider 3 basic configurations described as systems A, B, and C, and diagrammed in Figure 13 with variations to be described later.

The main difference in how to treat the tracking-control circuits is based on the availability of shutdown-control signal inputs to the converters and upon the characteristics of the converters themselves. System-A has shutdown-control signal inputs available, while system B has no shutdown control available for the +3.3V  $V_{I/O}$ , and system C has no shutdown control available on either the  $V_{I/O}$  or  $V_{CORE}$  supplies.

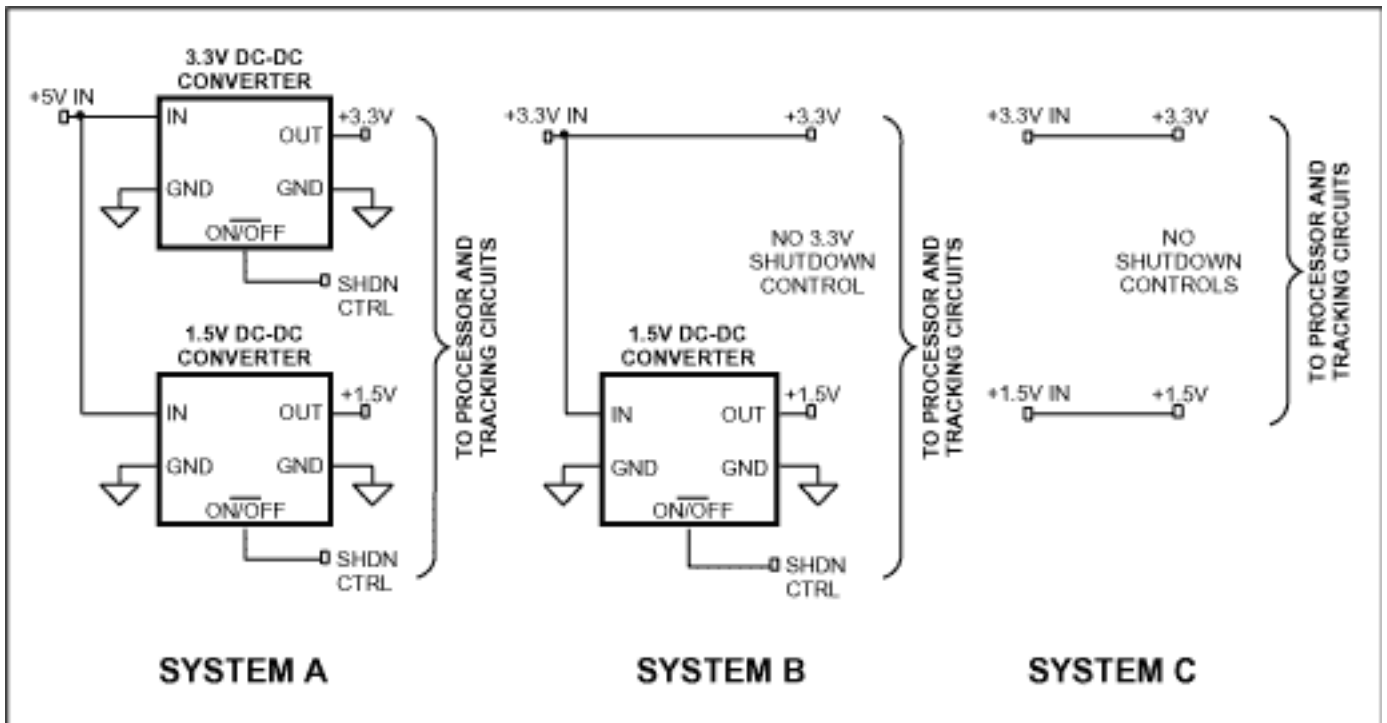


Figure 13. Three Basic Power System Source Configurations.

Systems B and C must include a series switch to interrupt and control one or more of the voltage sources. It has been previously mentioned that  $6.6\text{V}/\mu\text{s}$  is the maximum voltage rate of rise acceptable to the MAX5039/MAX5040 tracking controllers. The system processor specification may also restrict the maximum rate of rise for its  $V_{I/O}$  and  $V_{\text{CORE}}$  voltages. In these cases, the series switch must have the capability of controlling output voltage rate of rise. This is easily achieved when the tracking controller is augmented with a single MAX6820 power-supply sequencer IC plus a series MOSFET for each non-enabled supply.

In addition, we need knowledge of the DC-DC converter enable-controlled voltage rate of rise and over shoot, polarity of the enable control, and any enable sequencing requirements. Enable sequencing requirements may come about if the converter/regulator misbehaves when its output is backed from another voltage source at start up, or if the first converter to come up cannot support the entire system startup current including capacitor charging. In most cases it is desirable to delay the  $V_{\text{CORE}}$  enable signal by  $\sim 2\text{ms}$  after the  $V_{I/O}$  enable signal.

The power converters may be easily constructed using MAX1842 to meet required voltage rate of rise and overshoot characteristics, or modular converters may be purchased ready made. Some modular power converters like the Power Trends PT6600 series may require series MOSFET switching to control voltage rate of rise because of exhibited excessive enable-controlled output-voltage rate of rise and overshoot. Others like the DATEL LSN series exhibit nicely-controlled voltage rate of rise without overshoot, but may require staggered enable signals to ensure proper startup operation. The PT6600 series has positive-logic enable control, while the LSN series has negative-logic enable control. Table 1 lists some options.

### Table 1. Some Modular and Built-Up Converter Characteristics

| CONVERTER TYPE AND SERIES  | DISABLE SIGNAL POLARITY | ENABLE SEQUENCING REQUIRED      | ENABLE-CONTROLLED OUTPUT VOLTAGE RATE OF RISE                         | ENABLE-CONTROLLED OUTPUT VOLTAGE OVERSHOOT                            |
|----------------------------|-------------------------|---------------------------------|---|---|
| MAX1842 Discrete           | Negative                | Suggested with single R/C delay | Controlled  | Controlled  |
| DATEL LSN Series           | Positive                | Suggested with single R/C delay | Controlled  | Controlled  |
| Power Trends PT6600 Series | Negative                | Not applicable because of →     | Uncontrolled. Hardwire enable ON, and control input-voltage slew rate | Uncontrolled. Hardwire enable ON, and control input-voltage slew rate |

## Type-A System Configuration

A type-A system may be operated in a parallel configuration where all converters are driven from a single source as in Figure 14. The DATEL LSN series converters referenced exhibit friendly behavior to the ENABLE signal, but require an inverter in the ENABLE line. They may also benefit from a delay in the core-voltage converters so that the I/O voltage comes up before the core voltages. Simple and practical delay and inversion circuits are detailed in the Enable section.



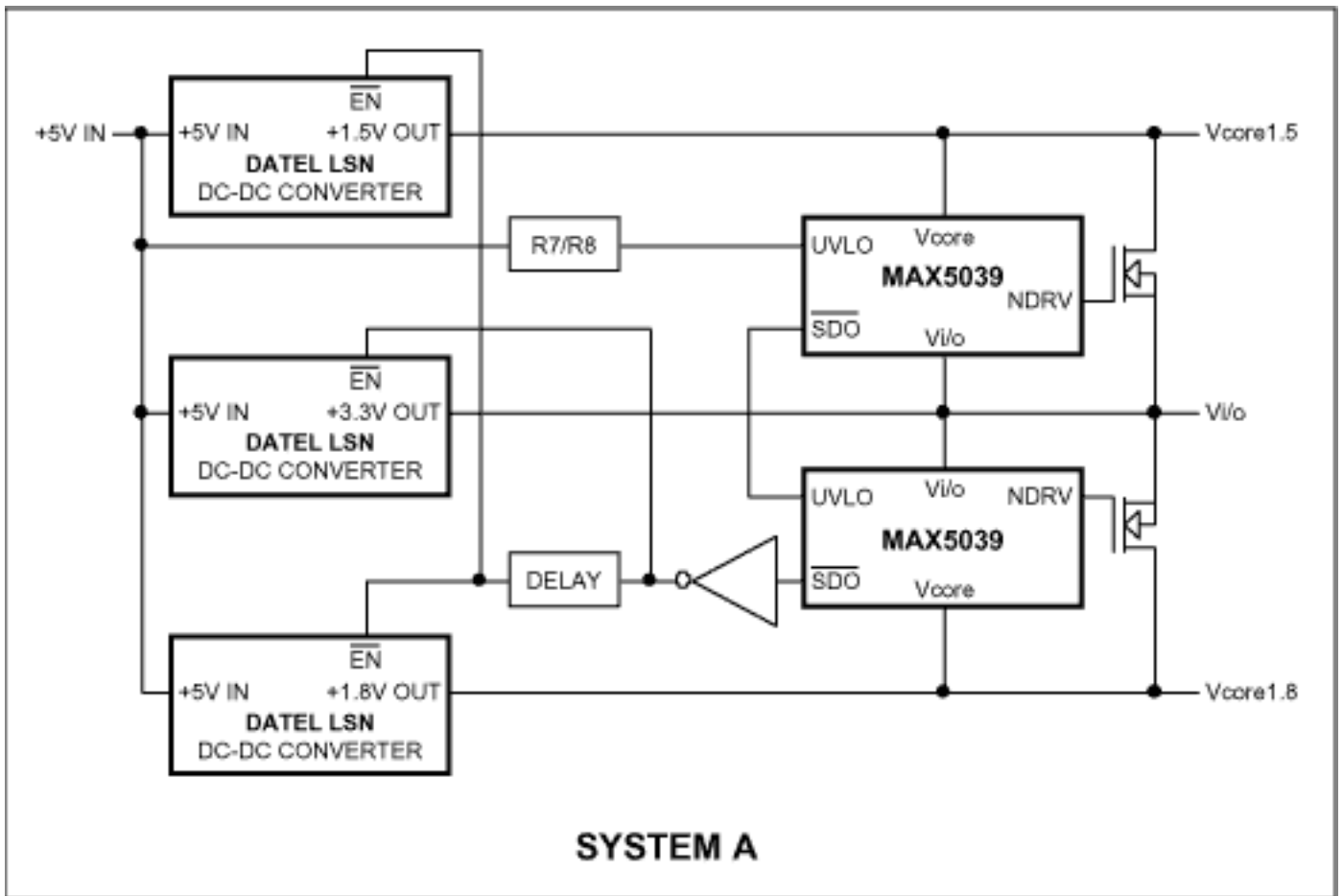


Figure 14. Parallel Type-A System also Illustrating Delayed and Inverted ENABLE.

Discrete converters built with the MAX1842 will operate in the circuit of Figure 15 without inverters in the enable line.

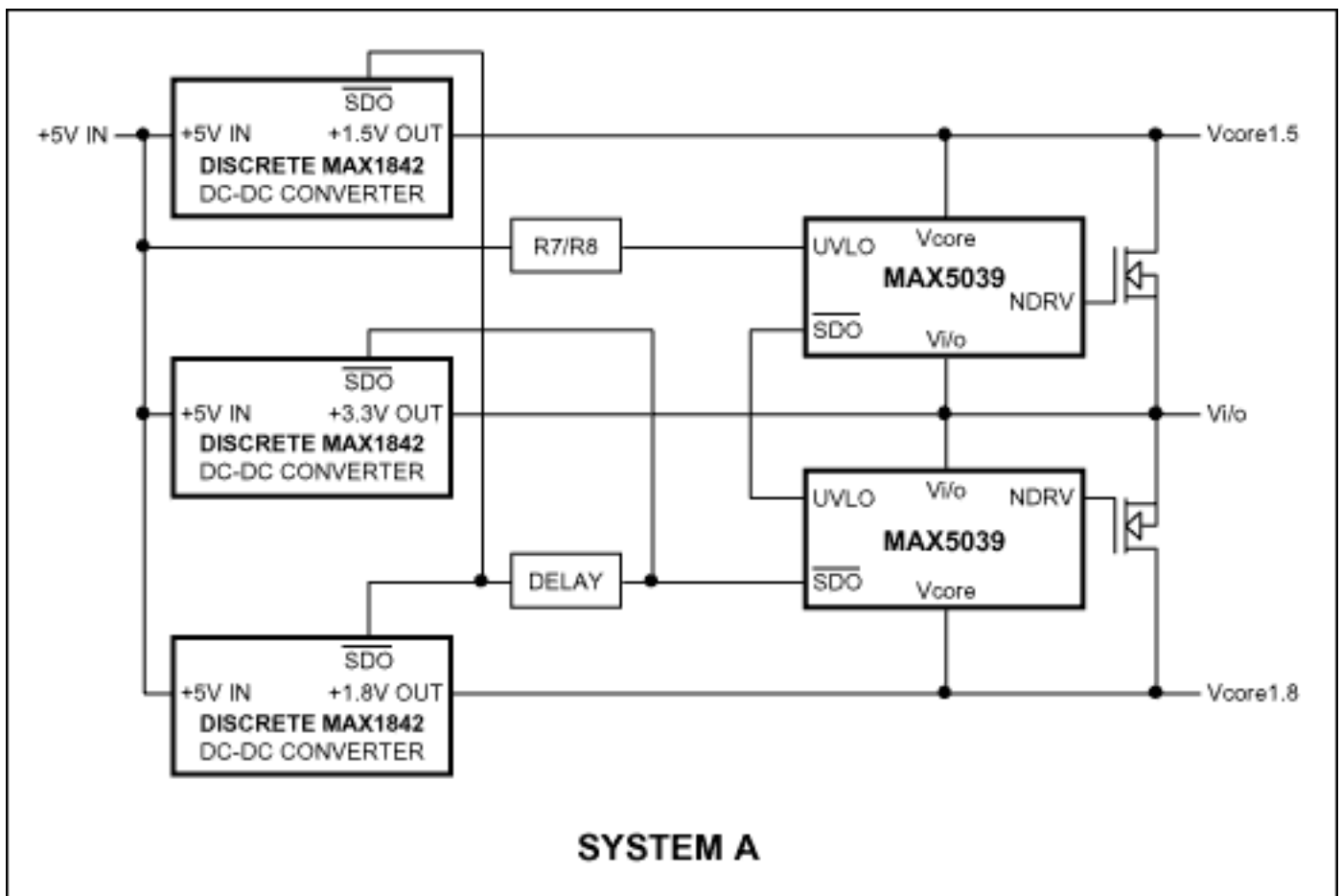


Figure 15. Parallel Type-A System with Discrete Converters.

## Type-B System Configuration

A type-B system is best operated in a cascade configuration as in Figure 16 if the regulators are not well behaved on an enable signal. In the cascade system, an external +3.3V supply is interrupted by a series MOSFET controlled by a MAX6820 IC; and the lower-voltage converters are powered from the output side of the series MOSFET. A capacitor is placed from series-MOSFET gate to ground to control the rate of rise of the interrupted +3.3V. The Power Trends PT6600 converters behave nicely with their ENABLE inputs are tied to their  $V_{IN}$  lines when the  $V_{IN}$  rate of rise is controlled by the series MOSFET. If the regulators used are well behaved at enable, the non-cascaded type B system in Figure 17 is suitable and places no extra stress on the 3.3V series MOSFET switch.

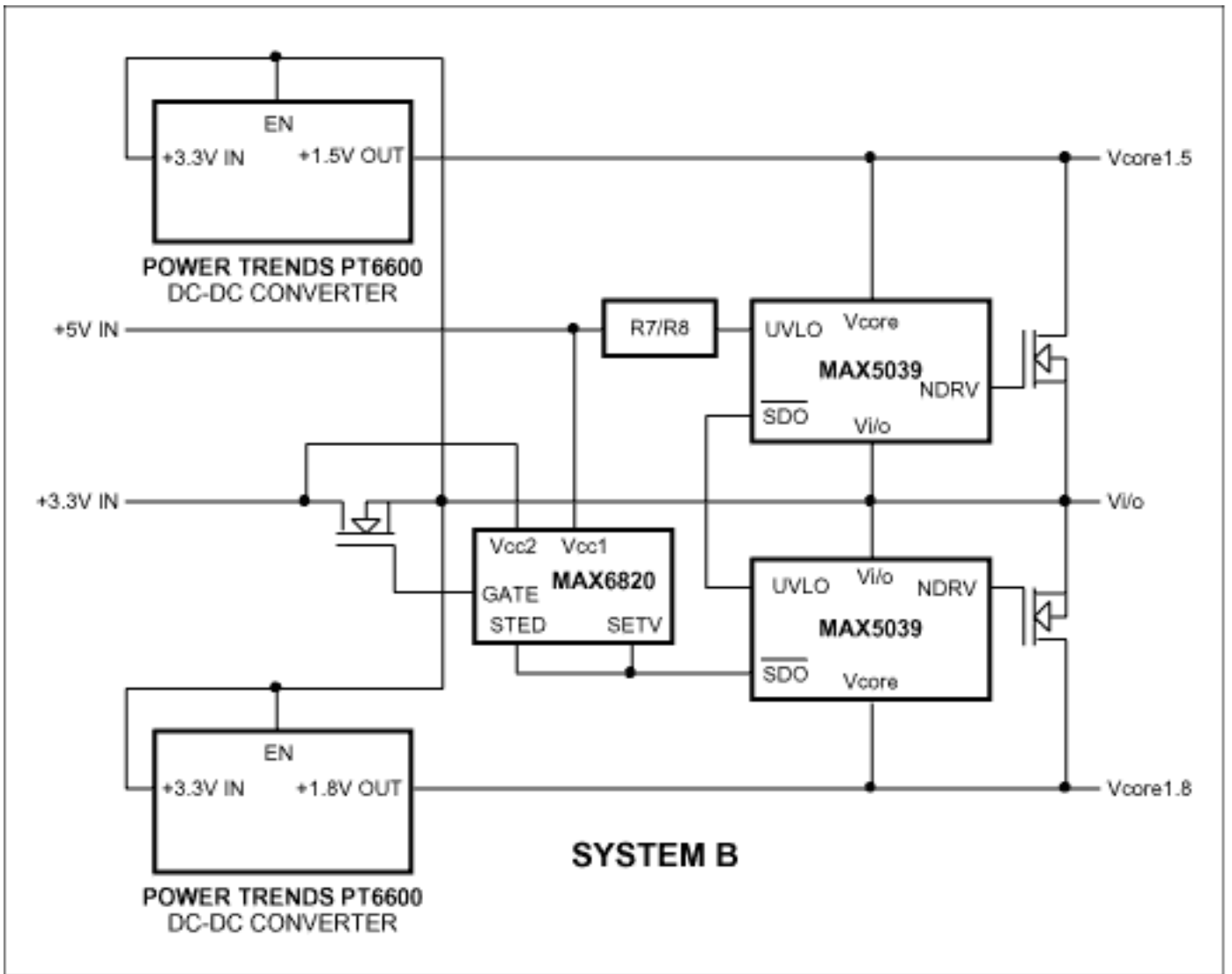


Figure 16. Cascade Type-B System.

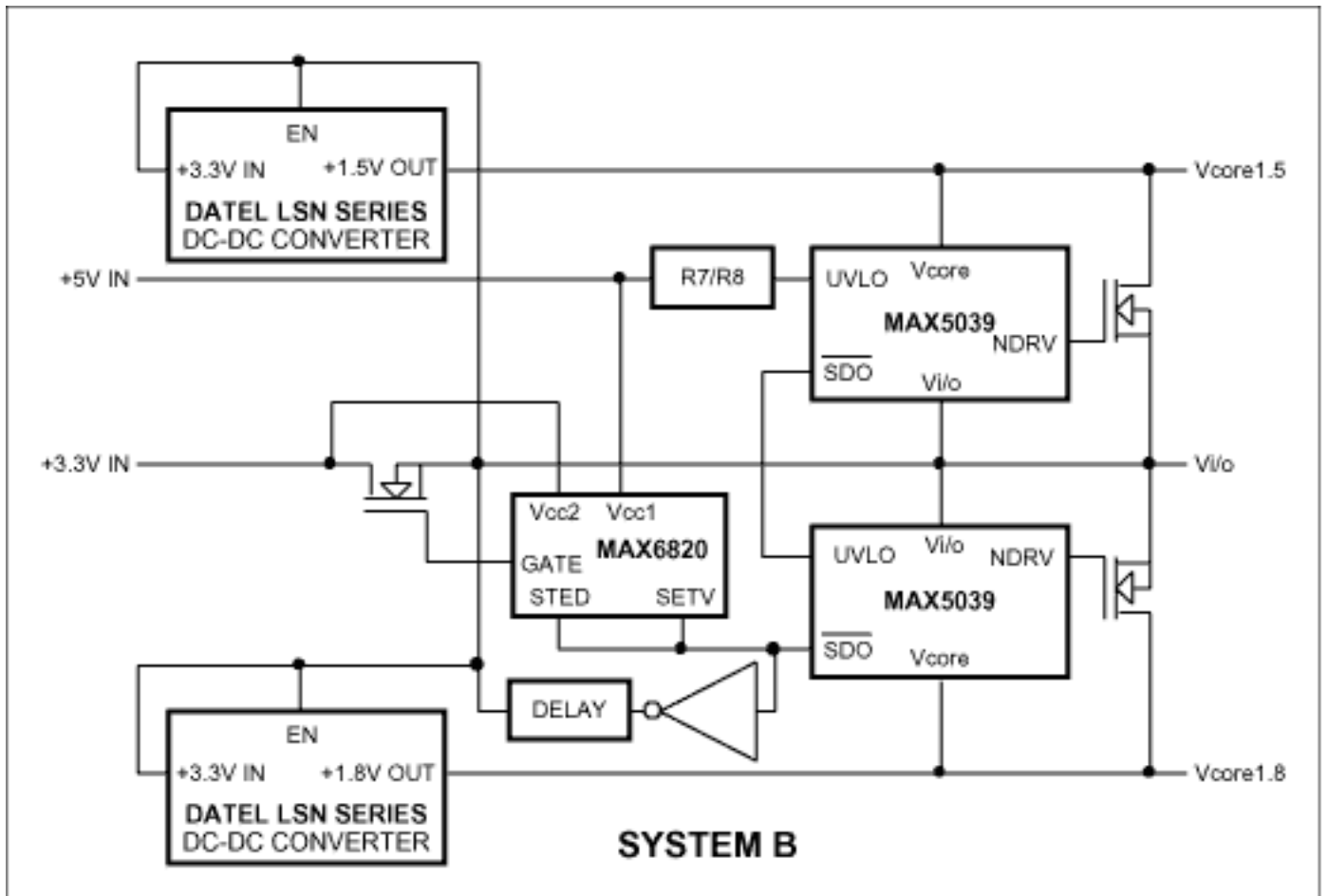


Figure 17. Parallel Type-B System.

## Type-C System Configuration

The type-C system requires a series MOSFET for each controlled voltage line because all voltage are always present, and no ENABLE control lines are available. All lines are interrupted and ramped up by a single MAX6820 supply sequencer IC as shown in Figure 18. A capacitor connected from gate to ground controls the voltage ramp rate. The MAX5039 /SDO\ output enables the MAX6820 at the appropriate time as controlled by the +5V input control line.

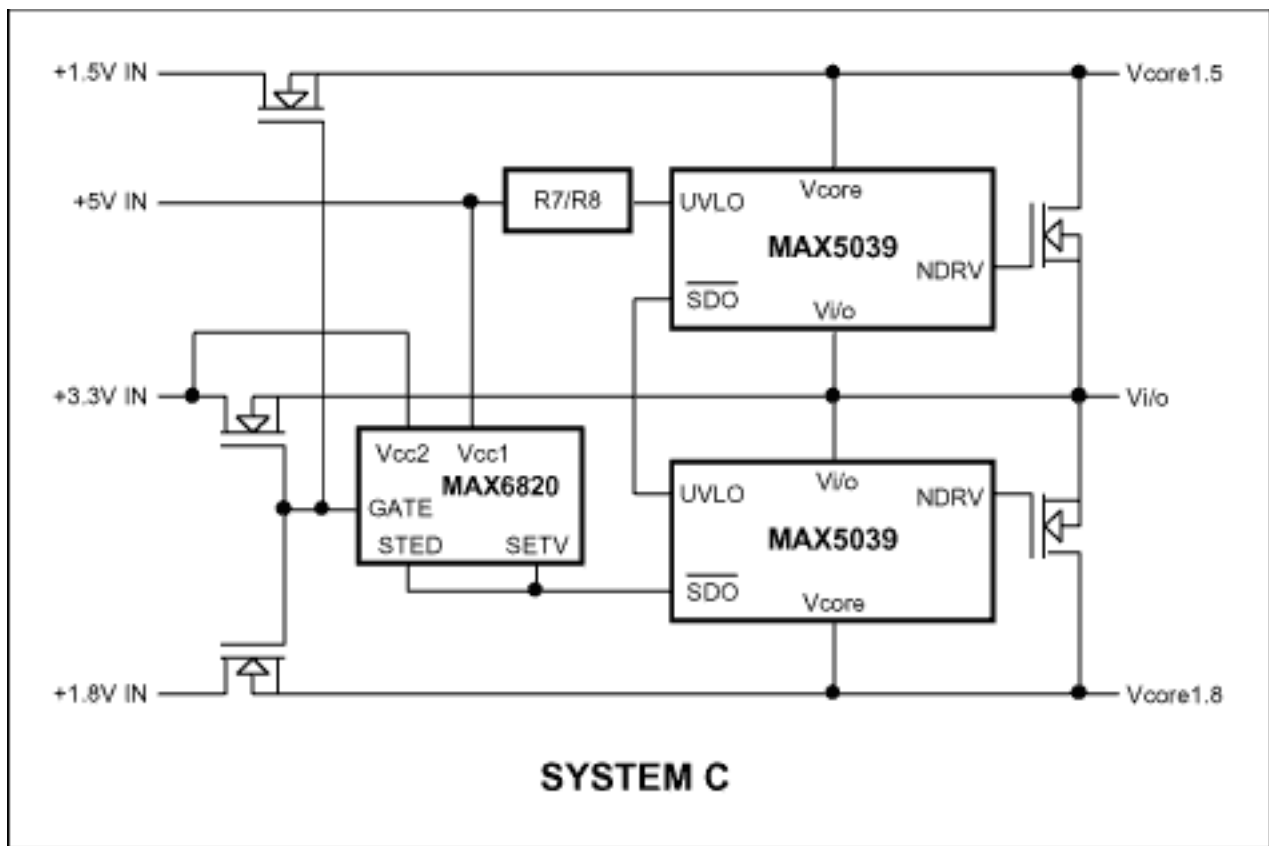


Figure 18. Type-C System.

## Enable Delay and Inversion Circuits

The MAX5039/MAX5040 provides an enable output, labeled /SDO\, for enabling/disabling external power converters or regulators. This output is negative-true disable, or positive-true enable. It will sink 1.5mA or source 1mA, so the outputs of multiple MAX5039s may not be collector-ORed together. Hence the daisy-chain connection previously shown in Figure 3 for a system using multiple MAX5039s.

It is recognized that this type of ENABLE output does not fit all regulator/converter ENABLE control signal requirements. Some converters have positive-true ENABLE inputs, while others have positive-true DISABLE inputs. Some, like the Power Trends PT6600 series, require an open-collector current-sinking DISABLE drive while others, like the DATEL LSN series, require a current-sourcing DISABLE drive. Converters built with the MAX1842 controller chip are well served directly by the MAX5039 /SDO\ current sinking/sourcing output.

Table 2 lists the enable/disable requirements of some commercially available modular converters.

Table 2 ENABLE Circuit Requirements

| PRODUCT | ENABLE SIGNAL MUST | DISABLE SIGNAL MUST | MAXIMUM APPLIED VOLTAGE |
|---------|--------------------|---------------------|-------------------------|
|---------|--------------------|---------------------|-------------------------|

|                            |                                     |                              |                          |
|----------------------------|-------------------------------------|------------------------------|--------------------------|
| DATEL LSN Series           | Open or LOW                         | Source 3mA @ $\geq 2.25V$    | Converter Input +Voltage |
| Power Trends PT6600 Series | Open or HIGH                        | Sink 0.5mA @ $\leq 0.35V$    | +5V                      |
| MAX1842                    | HIGH Source 1 $\mu$ A @ $\geq 2.0V$ | Sink 1 $\mu$ A @ $\leq 0.8V$ | Converter Input +Voltage |

Some practical enable/disable interface circuits that will meet almost any requirement are shown in Figure 19. Optional delayed-ON circuits are included. The third circuit provides a function specifically for Datel LSN series converters where the control input is positive-true DISABLE or negative-true ENABLE. With this converter, the unit is enabled if the input is open or grounded; and the input should not rise above the power input voltage level. As the MAX5039/MAX5040 /SDO\ output will source current when its output is high, an interface PNP transistor is best used at this interface when the converter is powered from +3.3V. The circuit is not required when the converter is powered from +5V. The circuit includes R2 to ensure that the converter DISABLE pin is driven high (disabled) during a period when the MAX5039 is not powered.

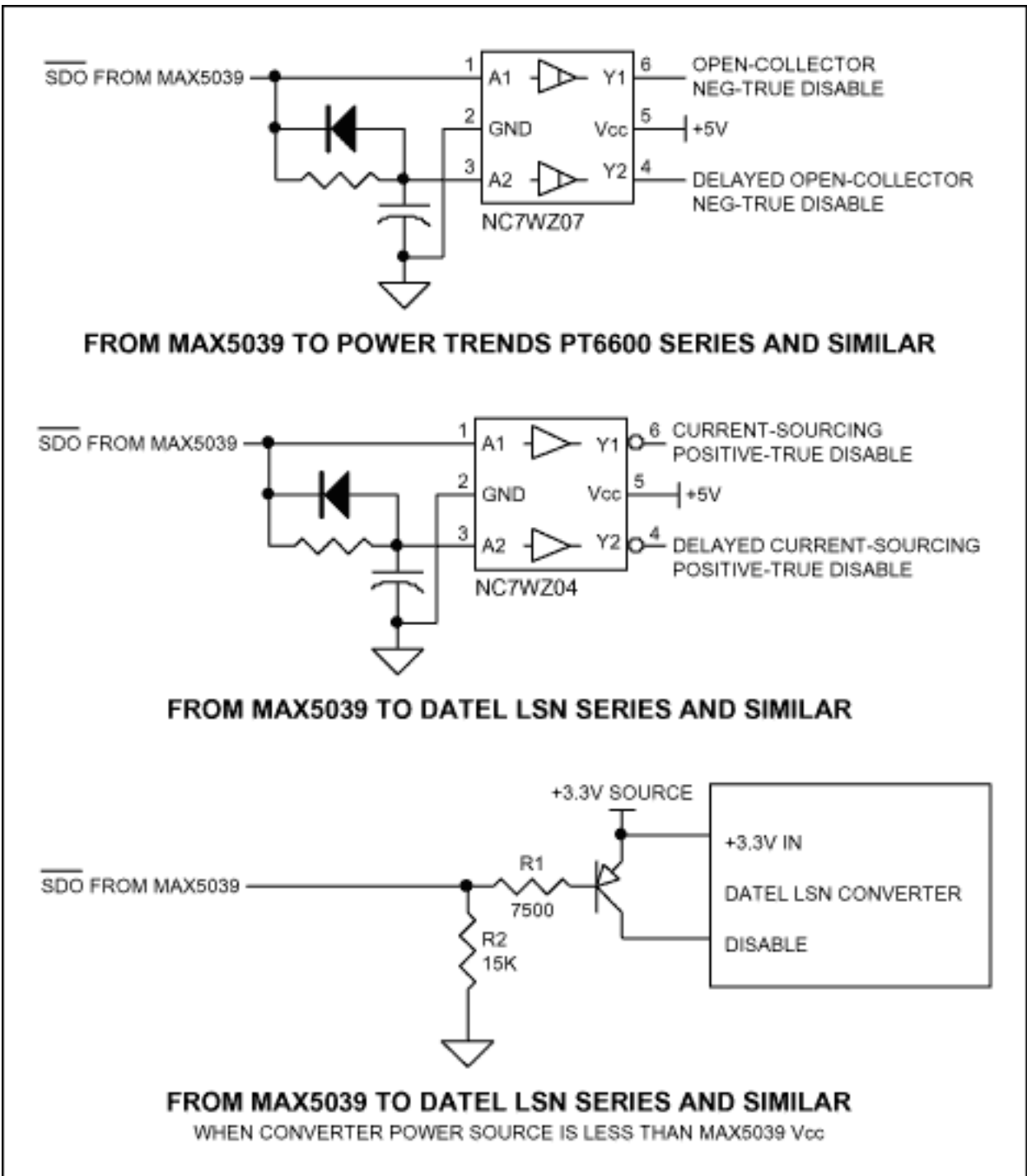


Figure 19. Enable Signal Interface Circuit Options including Delayed Options.

## Complete Type-A Circuits

Type-A system circuits have already been treated in Figures 2 & 3. Figure 20 shows a complete Type-A parallel system circuit constructed with discrete MAX1842 converters. These converters contain internal series and synchronous-rectifier MOS switches for minimum component count, and they can deliver 1A continuous or up to 2.8A peak output. Similar devices that deliver 2A and 3A continuous output are the MAX1644 and MAX1623. The larger soft-start capacitors on the two core-voltage converters provide for core voltage ramp-up delayed from the I/O voltage ramp-up, so no additional delays are needed.





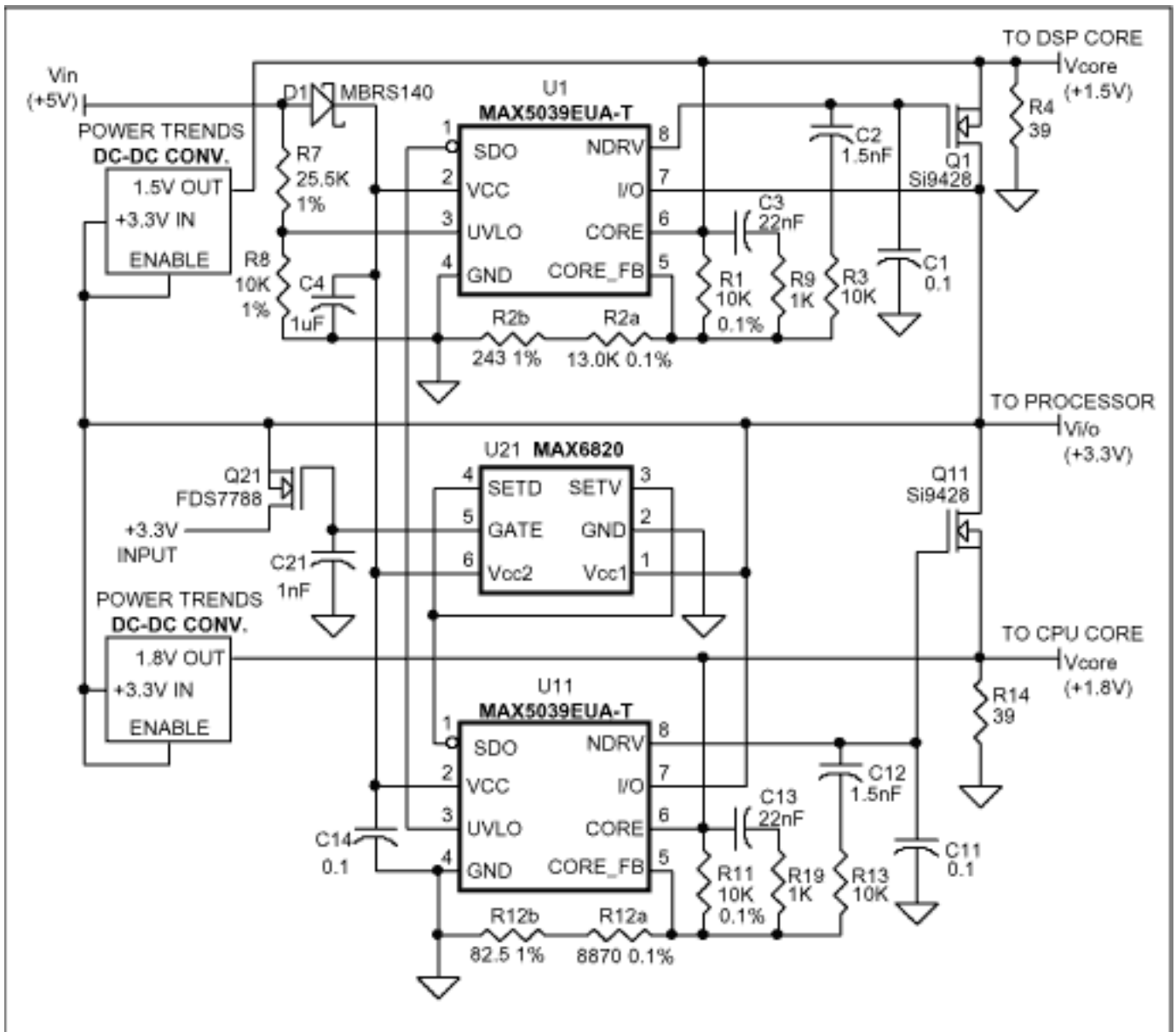


Figure 21. Complete Cascade Type-B System Circuit.

A complete circuit for a parallel type-B dual-tracking system is shown in Figure 22. The +3.3V output voltage rate of rise is controlled by C21, and the +1.5V and +1.8V rate of rise is controlled by the enable characteristics of the converters themselves. This circuit works well with Datal LSN series converters. With this configuration where startup control is by application of  $V_{IN}(+5V)$ , it is important that the 1.5V and 1.8V converter outputs reach final value within 10ms after application of  $V_{IN}(+5V)$  power.

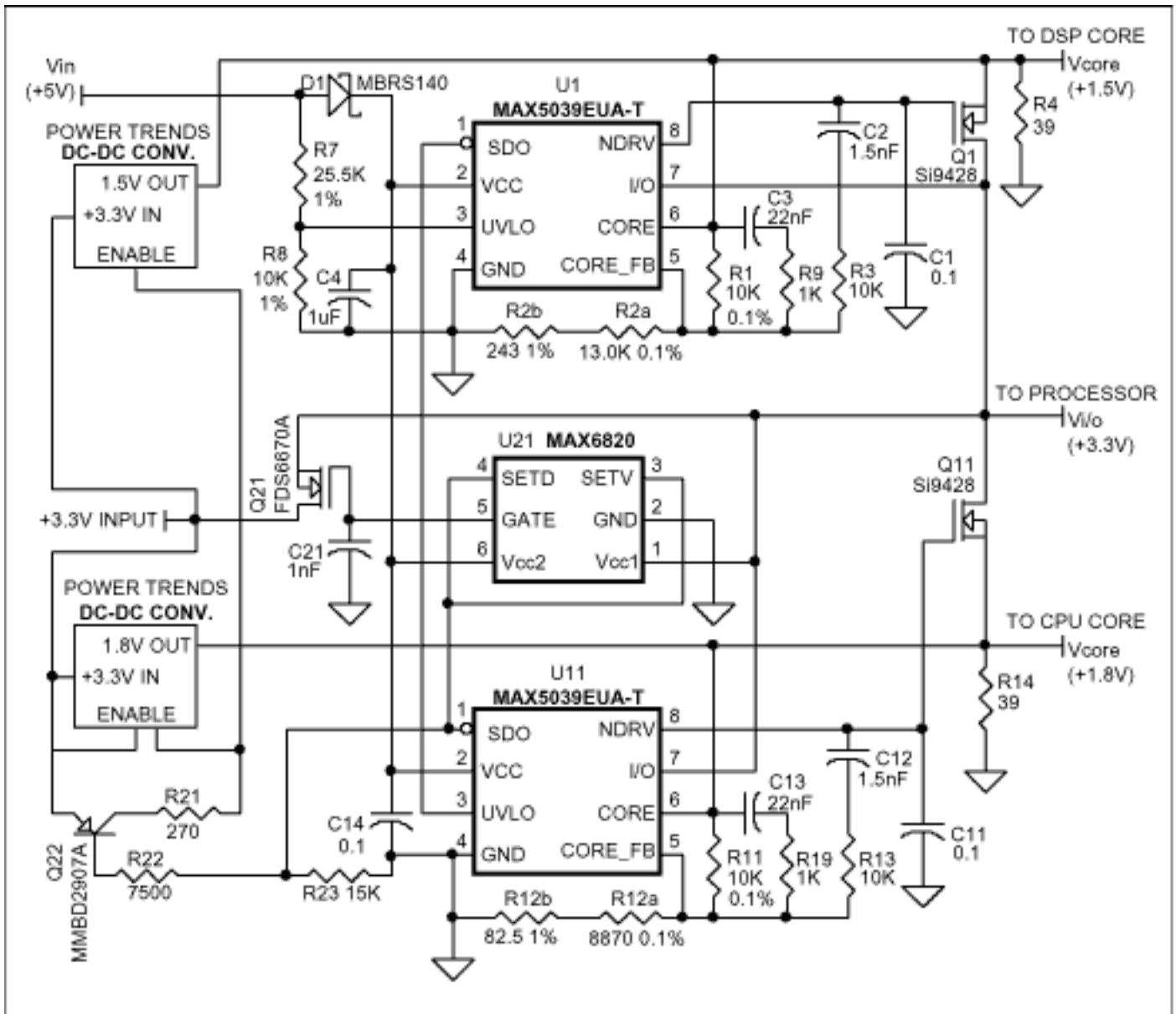


Figure 22. Complete Parallel Type-B System Circuit.

### Complete Type-C Parallel Circuit

A parallel type-C dual-tracking system circuit is shown in Figure 23. The output-voltage rate of rise for all three voltages is controlled by C21. With this configuration where startup control is by application of  $V_{IN} (+5V)$ , it is important that all three of the processor system voltages reach final value within 10ms after application of  $V_{IN} (+5V)$  power.

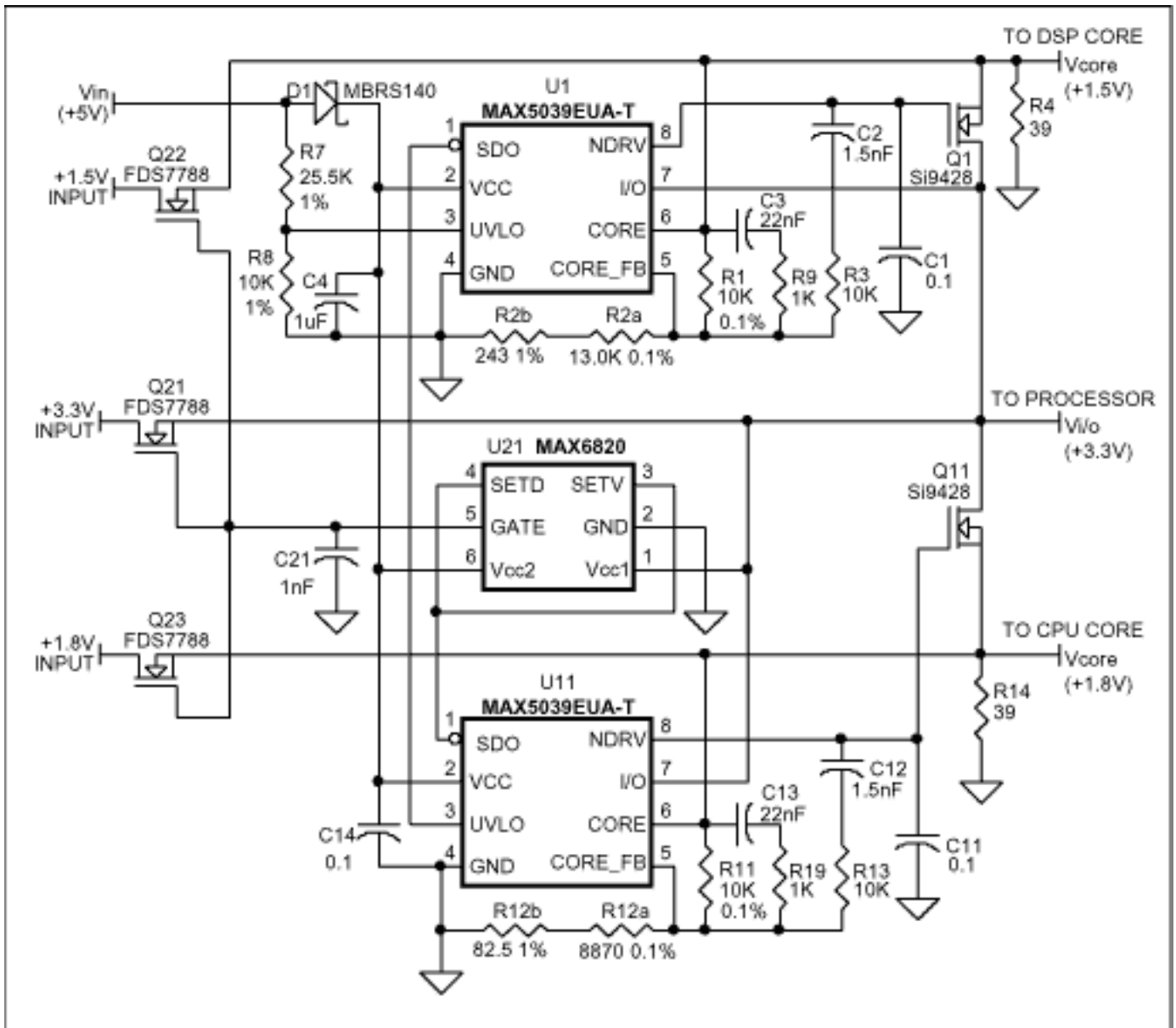


Figure 23. Complete Type-C System Circuit.

## Summary

The MAX5039/MAX5040 provides a simple and cost effective shunt voltage-tracking function for processor I/O and CORE voltages, yet introduces no series voltage/power loss in applications where the power sources can be electronically disabled/enabled.

When the supply-voltage sources cannot be individually enabled/disabled the addition of series MOSFET switches and a single MAX6820 (SOT23) voltage sequencer IC satisfies the additional control requirement.

Nearly any power-system voltage tracking requirement can be satisfied directly with one of the completely detailed circuits proposed, or a simple variation thereof, and nearly any enable/disable interface can be properly mechanized with one of the enable interface circuits proposed.

The Component-Selection Spreadsheet simplifies the process of tracking circuit design. Custom EV kits and technical assistance are available when appropriate.

## Reference

[1] This is accomplished by inserting a Schottky diode in series with the  $V_{CC}$  line after the UVLO sensing network as shown in Figures 2 & 3.

[2]  $V_{REGNOM}$  is the term used in the data sheet;  $V_{CT}$  is used here for brevity.

[3] The E96 series is the 100, 102, 105, 107 series; the E24 series is the 100, 110, 120, 130 series. There is also an E192 MIL-STD sequence that is the 100, 101, 102, 104 sequence, but it is uncommon.

[4] The data sheet erroneously suggests a minimum open-loop gain of 200.

[5] If  $V_{CT}$  should be selected very close to  $V_{REF}$ , say 0.9-1.0V, then one may wish to set  $R1 < 10k\Omega$ .

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## More Information

MAX1623: [QuickView](#) -- [Full \(PDF\) Data Sheet](#) -- [Free Samples](#)

MAX1644: [QuickView](#) -- [Full \(PDF\) Data Sheet](#) -- [Free Samples](#)

MAX1842: [QuickView](#) -- [Full \(PDF\) Data Sheet](#) -- [Free Samples](#)

MAX5039: [QuickView](#) -- [Full \(PDF\) Data Sheet](#) -- [Free Samples](#)

MAX5040: [QuickView](#) -- [Full \(PDF\) Data Sheet](#) -- [Free Samples](#)

MAX6820: [QuickView](#) -- [Full \(PDF\) Data Sheet](#) -- [Free Samples](#)